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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,087	08/21/2006	Woflgang Fey	AP 10889	4162

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EXAMINER	
AHMED, ENAM	
ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/590,087	FEY ET AL.	
	Examiner	Art Unit	
	ENAM AHMED	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non – Final

35 U.S.C. 102

a. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 25-30, 32, 35-36 and 38-39 are rejected under 35 U.S.C. 102(b) as being unpatentable over Hofsass et al. (U.S. Patent No. 5,522,040).

With respect to claim 25, the Hofsass et al. reference teaches transferring one or more error signals between at least one microprocessor chip or multiple processor .mu.C (1) (see fig. 1, 20 - Pulse Generator) and at least one further component (2) (see fig. 1, 4 – Watchdog circuit); and defining, for the transferring of error signals, a minimum pulse length that is independent of a clock frequency of the microprocessor chip or the multiple processor is defined, starting from a signal on an error line having a defined pulse length is interpreted as an error (column 3, lines 34-50) and (column 3, line 51 – column 4, line 32).

With respect to claim 26, the Hofsass et al. reference teaches wherein the further component is a mixed-signal module (column 3, lines 34-50) and (column 3, line 51 – column 4, line 32).

With respect to claim 27, the Hofsass et al. reference teaches wherein in the event of a sequence of errors with a distance between the errors that is smaller than the minimum pulse length, the time of the sequence of errors output over the at least one error line is extended with respect to the actual error sequence time (column 3, lines 34-50) and (column 3, line 51 – column 4, line 32).

With respect to claim 28, the Hofsass et al. reference teaches wherein the error signal in a chip, which receives the error signal of another chip or component, are not processed when the signals do not reach a minimum duration, and are processed when the minimum duration is reached or exceeded, and the signals are directed through at least one filter (column 3, lines 34-50) and (column 3, line 51 – column 4, line 32).

With respect to claim 29, the Hofsass et al. reference teaches wherein at least one watchdog time window (17) is predetermined in the integrated circuit or in the further component (2), within which at least one artificially produced error signal or error signal pattern is generated and tested so that the error detection circuits become self-testable (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

With respect to claim 30, the Hofsass et al. reference teaches wherein the watchdog time window (17) has a delay time TWindowDelay, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time TWindowDelay (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

With respect to claim 32, the Hofsass et al. reference teaches wherein the time window TWindowDelay is set in the further component (2) by way of the interface (5) connected to chip (1) (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

With respect to claim 35, the Hofsass et al. reference teaches wherein inside the chip (1) that sends error signals, the error signals are extended and/or output with delay one after the other through the error line (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

With respect to claim 36, the Hofsass et al. reference teaches wherein a test of the at least one error line (3, 4) is performed with the aid of an interface (5) (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

With respect to claim 38, the Hofsass et al. reference teaches wherein the pulse width TMin is set to a value of at least 30 nanoseconds approximately (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

With respect to claim 39, the Hofsass et al. reference teaches at least one microprocessor chip or multiple processor microcontroller (1) or microprocessor module (see fig. 1,Microcomputer); at least one additional separate component (2) having separately arranged power elements (see fig. 1, 4 – Watchdog circuit); and one or more pulse extending devices or signal delaying devices for outputting error pulses (6, 6') one after another through at least one error line (3, 4) (see fig. 1, 20 - Pulse Generator), (column 3, lines 34-50) and (column 3, line 51 – column 4, line 32).

35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31, 33-34 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsass et al. (U.S. Patent No. 5,522,040) in view of El Malki (U.S. Patent No. 6,044,068).

With respect to claim 31, all of the limitations of claim 30 have been addressed. The Hofsass et al. reference does not teach wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal or error signals of the at least

one error line (3, 3'). The El Malki reference teaches wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal or error signals of the at least one error line (3, 3') (column 8, line 61 – column 9, line 4). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and El Malki to incorporate wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal or error signals of the at least one error line (3, 3') into the claimed invention. The motivation for wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal or error signals of the at least one error line (3, 3') is for improved system performance.

With respect to claim 33, all of the limitations of claim 30 have been addressed. The Hofsass et al. reference does not teach wherein a condition TWindowDelay is satisfied in excess of the filter time TFilter. The El Malki reference teaches wherein a condition TWindowDelay is satisfied in excess of the filter time TFilter (column 11, lines 32-44). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and El Malki to incorporate wherein a condition TWindowDelay is satisfied in excess of the filter time TFilter into the claimed invention. The motivation for wherein a condition TWindowDelay is satisfied in excess of the filter time TFilter is for improved system performance.

With respect to claim 34, all of the limitations of claim 30 have been addressed. The Hofsass et al. reference does not teach wherein the delay TWindowDelay approximately corresponds to twice the time TFilter. The El Malki reference teaches wherein the delay TWindowDelay approximately corresponds to twice the time TFilter (column 8, line 61 – column 9, line 4. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and El Malki to incorporate wherein the delay TWindowDelay approximately corresponds to twice the time TFilter into the claimed invention. The motivation for wherein the delay TWindowDelay approximately corresponds to twice the time TFilter is for improved system performance.

With respect to claim 37, all of the limitations of claim 25 have been addressed. The Hofsass et al. reference does not teach wherein the error signals are filtered by filters (7, 7') with a defined filter time TFilter. The El Malki reference teaches wherein the error signals are filtered by filters (7, 7') with a defined filter time TFilter (column 8, line 61 – column 9, line 4). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and El Malki to incorporate wherein the error signals are filtered by filters (7, 7') with a defined filter time TFilter into the claimed invention. The motivation for wherein the error signals are filtered by filters (7, 7') with a defined filter time TFilter is for improved system performance.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsass et al. (U.S. Patent No. 5,522,040) in view of McCormick (U.S. Patent No. 5,488,872).

With respect to claim 40, all of the limitations of claim 39 have been addressed. The Hofsass et al. reference does not teach one or more filters (7, 7') for filtering the error signals transferred through the error lines (3, 4). The McCormick reference teaches one or more filters (7, 7') for filtering the error signals transferred through the error lines (3, 4) (column 5, lines 39-49). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and McCormick to incorporate one or more filters (7, 7') for filtering the error signals transferred through the error lines (3, 4) into the claimed invention. The motivation for one or more filters (7, 7') for filtering the error signals transferred through the error lines (3, 4) is for improved system performance.

Claims 41 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsass et al. (U.S. Patent No. 5,522,040) in view of McCormick (U.S. Patent No. 5,488,872).

With respect to claim 41, the Hofsass et al. reference teaches at least one microprocessor chip or multiple processor microcontroller (1) (see fig. 1,Microcomputer); at least one additional component (2) having separately arranged power elements (see fig. 1, 4 – Watchdog circuit), wherein one or more error signal is transferred between the at least one microprocessor chip or multiple processor .mu.C (1) and the at least one additional component (2) (see fig. 1, 20 - Pulse

Generator), (column 3, lines 34-50) and (column 3, line 51 – column 4, line 32). The Hofsass et al. reference does not teach and one or more filter (7, 7') for filtering error pulses (6, 6') through at least one error line (3, 4). The McCormick reference teaches and one or more filter (7, 7') for filtering error pulses (6, 6') through at least one error line (3, 4) (column 5, lines 39-49). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and McCormick to incorporate one or more filter (7, 7') for filtering error pulses (6, 6') through at least one error line (3, 4) into the claimed invention. The motivation for one or more filter (7, 7') for filtering error pulses (6, 6') through at least one error line (3, 4) is for improved system performance.

With respect to claim 45, the Hofsass et al. reference teaches wherein the microprocessor chip (1) or the additional component comprises at least one watchdog window circuit (50) (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

With respect to claim 46, the Hofsass et al. reference teaches wherein the watchdog window circuit (50) predefines a watchdog time window (17), and the watchdog time window (17) has a delay time TWindowDelay, and the time window, in which at least one error signal or error signal pattern is expected, remains open until the expiry of the delay time TWindowDelay (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsass et al. (U.S. Patent No. 5,522,040), McCormick (U.S. Patent No. 5,488,872) in view of El Malki (U.S. Patent No. 6,044,068).

With respect to claim 42, all of the limitations of claim 41 have been addressed. The Hofsass et al. reference does not teach wherein the filter (7, 7') is configured as a digital forward/backward counter. The El Malki reference teaches wherein the filter (7, 7') is configured as a digital forward/backward counter (column 10, lines 11-26). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and El Malki to incorporate wherein the filter (7, 7') is configured as a digital forward/backward counter into the claimed invention. The motivation for wherein the filter (7, 7') is configured as a digital forward/backward counter is for improved system performance.

Claims 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsass et al. (U.S. Patent No. 5,522,040), McCormick (U.S. Patent No. 5,488,872) in view of Cheney et al. (U.S. Patent No. 5,333,301).

With respect to claim 43, all of the limitations of claim 41 have been addressed. The Hofsass et al. reference does not teach wherein the chips or components are interconnected by at least one bus (5) and at least one error line (3, 4). The Cheney et al. reference teaches wherein the chips or components are interconnected by at least one bus (5) and at least one error line (3, 4) (column 1, lines 57-65). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and Cheney et al. to incorporate wherein the chips or components are interconnected by at least one bus (5) and at least one error line (3, 4) into the claimed invention. The motivation for wherein the chips or

components are interconnected by at least one bus (5) and at least one error line (3, 4) is for improved system performance.

With respect to claim 44, the Hofsass et al. reference teaches wherein the circuit includes hardware test structures, with the aid of which a test of the at least one error line (3, 4) can be performed using an interface (5) (column 2, line 62 – column 3, line 6), (column 3, lines 43-50) and (column 4, lines 2-32).

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofsass et al. (U.S. Patent No. 5,522,040), McCormick (U.S. Patent No. 5,488,872) in view of El Malki (U.S. Patent No. 6,044,068).

With respect to claim 47, all of the limitations of claim 45 have been addressed. The Hofsass et al. reference does not teach wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal(s) of the at least one error line (3, 3'). The El Malki reference teaches wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal(s) of the at least one error line (3, 3') (3, 3') (column 8, line 61 – column 9, line 4). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Hofsass et al. and El Malki to incorporate wherein the delay time TWindowDelay is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal(s) of the at least one error line (3, 3') into the claimed invention. The motivation for wherein the delay time TWindowDelay

is longer than the filter time TFilter of the filter(s) (7, 7') processing the error signal(s) of the at least one error line (3, 3') is for improved system performance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman, can be reached on 571-272-3644.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

11/21/09

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Primary Examiner, Art Unit 2112